CBCS Scheme

USN | | | | | | | | | | |

15EE35

Third Semester B.E. Degree Examination, June/July 2017
Digital System Design

Time: 3 hrs. Max. Marks: 80

Note: 1. Answer any FIVE full questions, choosing one full question from each module.
2. Assume Missing Data if any suitably

Module-1

1 a. Write the truth table of the logic circuit having 3 inputs: A, B and C and an output $Y = AB\overline{C} + \overline{A}BC + ABC$. Also simplify the Boolean expression and implement the logic circuit using NAND gates only. **(06 Marks)**

b. Using Quine – McCluskey method, simplify: $f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$. **(10 Marks)**

OR

2 a. Define Canonical Minterm formula and Canonical maxterm formula with an example for each. **(04 Marks)**

b. Simplify the Boolean expression using 'd' as MEV for $f(a, b, c, d) = \sum m(2, 3, 4, 5, 8, 9, 10, 11, 13, 15)$ **(06 Marks)**

c. Design a three input, A, B and C and one output ; 'Y'; minimal, two level gate combinational circuit which has an output equal to 'zero' when majority of its inputs are at logic '1'. **(06 Marks)**

Module-2

3 a. Design a comparator to check if two N-bit numbers are equal. Configure this using cascaded stages of 1 – bit comparator. **(04 Marks)**

b. Write the compressed truth table for a 4 to 2 line priority encoder with a valid output and simplify the same using K-Map. Design the logic circuit as well. **(06 Marks)**

c. Implement the following Boolean function using a 4:1 MUX with A and B as select lines $Y = f(A, B, C, D) = \sum m(0, 1, 2, 4, 6, 9, 12, 14)$. **(06 Marks)**

OR

4 a. Write a short note on 4-bit parallel Adder. **(04 Marks)**

b. Using active high output 3:8 line decoder, implement the following functions
$f_1(A, B, C, D) = \sum m(0, 1, 2, 5, 7, 11, 15)$
$f_2(A, B, C, D) = \sum m(1, 3, 4, 11, 13, 14)$ **(06 Marks)**

c. Design an 8:1 MUX Tree using only 2:1 multiplexers. **(06 Marks)**

Module-3

5 a. With a neat logic diagram, explain working of a Master slave JK Flip-Flop along with waveforms. Also brief about Race-around condition. **(08 Marks)**

b. Convert a T – Flip-Flop to a D – Flip-Flop. **(04 Marks)**

c. Write a short note on shift Registers. **(04 Marks)**

OR

6 a. Design Synchronous Mod – 6 counter using SR Flip-Flops. **(08 Marks)**

b. Compare Asynchronous and Synchronous counters. **(04 Marks)**

c. Explain working of a 4-bit binary ripple down counter configured using negative edge triggered JK Flip-Flop with timing diagram. **(04 Marks)**

Module-4

7 a. Explain Melay and Moore models with neat block diagrams. **(04 Marks)**

b. Analyse the synchronous circuit of the Fig Q7(b) shown below.

i) Write down excitation and output functions.

ii) Form the excitation and state tables

iii) Give description of the circuit operation. **(12 Marks)**

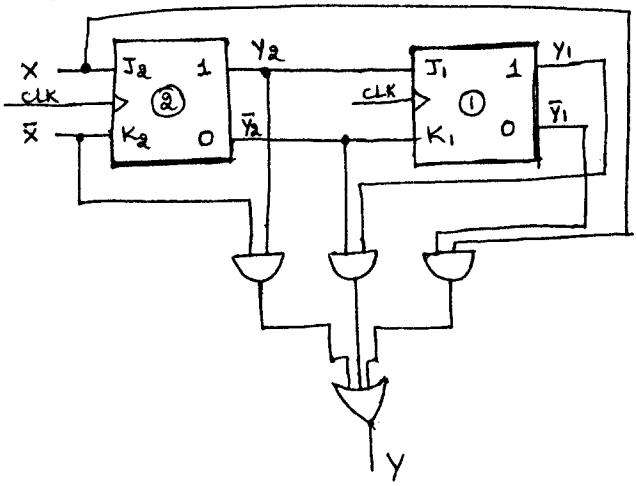

Fig Q7(b)

OR

8 a. Define state, present state, state diagram and state table. **(04 Marks)**

b. Construct Moore and Melay model state diagrams to detect input sequence 10110. When the input pattern is detected, output 'Z' is asserted HIGH. **(06 Marks)**

c. Construct a state diagram for synchronous decade UP/DOWN counter. The mode control 'M' decides the pattern of counting operation. When M = 0 'Counter counts UP and when M = 1; the counter counts DOWN. When the counter reaches terminal count Y = 1 (for UP count) and Z = 1 (for DOWN count). Label the state diagram in M/YZ mode. **(06 Marks)**

Module-5

9 a. Mention styles/types of HDL description. Explain behavioral type with half adder example in both VHDL and verilog. **(08 Marks)**

b. Compare VHDL and verilog. **(04 Marks)**

c. Explain verilog data types. **(04 Marks)**

OR

10 a. Tabulate Rotate operators used in HDL with example operand A = 1110. **(08 Marks)**

b. Draw the block diagram of 3-bit carry look ahead adder. Write verilog code for the same. **(08 Marks)**

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